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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/043,516	01/11/2002	Johann Fuhrmann	DE 01007	8286

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EXAMINER

HU, SHOUXIANG

ART UNIT	PAPER NUMBER
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2811

DATE MAILED: 12/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/043,516

Applicant(s)

FUHRMANN ET AL.

Examiner

Shouxiang Hu

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 October 2003.
- 2a) ☒ This action is FINAL. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
- a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s) _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claim Objections

1. Claims 1-21 are objected to because of the following informalities and/or defects:

The amendment to the claims filed on 10-20-03 does not comply with the requirements of 37 CFR 1.121(c) because it fails to follow the requirement that the text of any added subject matter (for example, the "wherein" phrase in the last two lines of the amended claim 1) must be shown by underlining the added text.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-21 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Newly amended claim 1 recites the subject matter that "wherein the signal-generating unit (40) and the evaluation unit (70) are integral parts of the semiconductor chip". However, full support for it cannot be found in the original disclosure, which (see page 1, lines 1-9, and page 5, lines 14-20; also see

Figs. 1 and 2) shows that, while the capacitor tracks (20 and 25) are integral parts of the chip, the signal-generating unit (40) and the evaluation unit (70) are situated outside the chip (10; as shown in Fig. 2).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2 and 6-21, insofar as being in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 102(b) as being anticipated by Hierold et al. ("Hierold"; DE 19738990A1; of record).

Hierold discloses an electric or electronic circuit arrangement and a method of protecting a electronic circuit arrangement thereof (Figs. 1, 2, 5 and 7, particularly Fig. 5), comprising: a layered carrier substrate (2) of a semiconducting or insulating material; at least one integrated circuit constituted by at least two spaced and lithographically applied conductor tracks (20₁, see Fig. 5 in view of Fig. 1) on the carrier substrate (2); at least one dielectric shielding layer (all insulating layers above the substrate 2) including an inherent insulation layer and/or passivation layer (the layer between the substrate 2 and the layer 40) and/or a further protective layer (the insulating layer(s) above the layer 40) situated between the conductor tracks (20₁) and/or laterally with respect to the conductor tracks (20₁) and/or on the conductor tracks (20₁), provided for protecting the

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integrated circuit from external influences so that the integrated circuit has a specific, particularly lateral and/or particularly parasitic capacitance (C) determined by the dielectric shielding layer, characterized in that at least one signal-generating unit (51) including at least an oscillator unit is connected to the contact terminals (see Fig. 5) of the integrated circuit, the output frequency (f) of which unit is substantially determined by the specific capacitance, in that the signal-generating unit (51) precedes at least a first counting unit (521) which is clocked at the output frequency (f) of the signal-generating unit (51), in which counting unit an actual value count can be determined after a predetermined temporal counting period, in that at least a second counting unit (53) clocked at a reference frequency is provided, in which counting unit a nominal value count can be determined after the predetermined temporal counting period, in that the first counting unit (51) and the second counting unit (53) precede at least one comparator unit (54) for comparing the actual value count with the nominal value count, while the functions of the integrated circuit can be blocked and/or locked and/or interrupted temporarily or permanently in the case of an error indication which occurs when the actual value count is compared with the nominal value count.

Regarding claim 2, the conductor tracks (20₁) in Hierold are at least sectionally arranged parallel to each other and/or in a meandering intermeshing configuration (see Fig. 5).

Regarding claims 6 and 20, it is noted that the signal-generating unit (51) in Hierold includes an oscillator, which normally inherently comprises at least one oscillator circuit consisting of at least one capacitive unit including a capacitor, and at

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least one resistive unit including a resistor, and/or at least one oscillator circuit consisting of at least one capacitive unit including a capacitor, and at least one inductive unit including a coil.

Regarding claims 7 and 13, a differential evaluation unit is naturally constituted by the first counting unit, the second counting unit and the comparator unit in Hierold.

Regarding claim 10, the arrangement in Hierold further includes a coding unit (522), which manifests that the first counting unit and/or the second counting unit are/is naturally formed on a digital basis.

Regarding claim 11, the arrangement of Hierold is for a chip card or smart card.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 3-5, as being best understood in view of the above claim objections, are rejected under 35 U.S.C. 103(a) as being unpatentable over Hierold et al. ("Hierold"; DE 19738990A1; of record).

The disclosure of Hierold is discussed as applied to claims 1, 2 and 6-15 above.

Regarding claim 3, it is noted that the mutual distance between the conductor tracks is in an art-recognized result-effective parameter of importance subject to routine

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experimentation and optimization; and that the recited micrometer range is well with the art-recognized normal range for the mutual distance between capacitor electrodes.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make the circuit arrangement of Hierold with the distance between the conductor tracks being in the micrometer range, so that a circuit arrangement with optimized performance would be obtained, because it has been held that "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Regarding claims 4 and 5, it is noted that silicon oxide and opaque resin are each among art-recognized insulating passivation materials commonly used for reliably and/or invisibly protecting IC devices, as evidenced in the prior art such as Daum (US 5,821,582; see col. 3, lines 32-33) and/or Ban et al. (US 6,060,773; see col. 1, lines 22-24).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make the circuit arrangement of Hierold with the dielectric shielding layer being formed of silicon oxide or opaque resin, so that an IC device with reliable and/or invisible protection would be obtained.

Response to Arguments

5. Applicant's arguments filed on 12/20/03 have been fully considered but they are not persuasive.

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Applicant's main arguments include that the applied prior art reference fails to teach the claimed subject matter that "the signal-generating unit (40) and the evaluation unit (70) are integral parts of the semiconductor chip". However, as explained in the claim rejections under 35 U.S.C 112 set forth above in this Office action, such subject matter is not supported by the original disclosure.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is (703) 306-

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5729. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

SH
December 16, 2003



SHOUXIANG HU
PRIMARY EXAMINER